

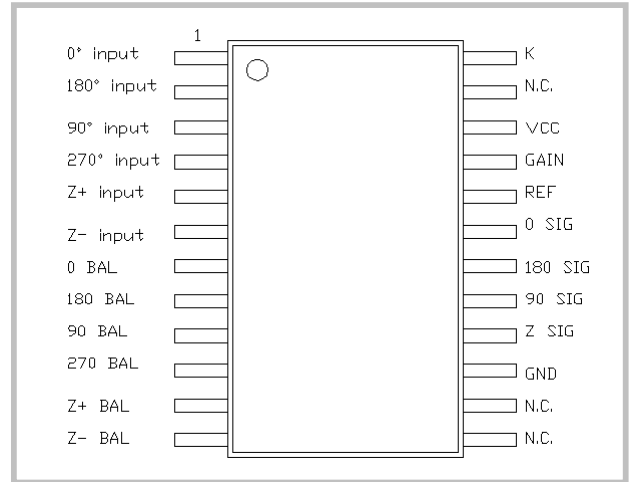
ANALOG SIGNAL PROCESSOR

ET2010

PRELIMINARY DATA SHEET

FEATURES

- Single supply operation
- Handles Sine/Cosine inputs from DC to 125KHz
- Photodiode input photocurrent range from 100nA
- Adjustable gain
- DC offset adjustable at each output
- Interfaces directly with ET2015 or ET2024 Interpolation devices



See pin descriptions on last sheet.

This part is available in a 24 lead TSSOP package, or as die.

Package	Suffix
24 Lead TSSOP	-TSS
Die	-C

DESCRIPTION

The ET2010 ASP is a monolithic bipolar ASIC designed to transform nanoamp-level differential photocurrents into 1Vpp sinewaves that are suitable for interpolation. A gain adjustment is provided that affects all channels in concert. Separate balance adjustments are provided for each output, for centering the waveforms on the reference voltage. In applications where the photocurrents are generated in phased-array photodiodes, the balance adjustments are generally not needed. In these cases, the BAL pins should be connected to GND. In most encoder designs, the LED optical output level changes with supply voltage, temperature, and age. This causes corresponding changes in the photocurrent signal levels. The ASP rejects these variations in the input signals, resulting in output levels that are stable over time, temperature, and supply voltage. In practice, the maximum usable gain setting may be limited by noise considerations. The comparators in Interpolation ASIC's have a minimal amount of hysteresis, and care must be taken that the noise is well below the hysteresis value. If necessary, the noise can be reduced by lowering the photodiode capacitance or by rolling off the ASP outputs with RC filters.

Preliminary Data – Subject to Change

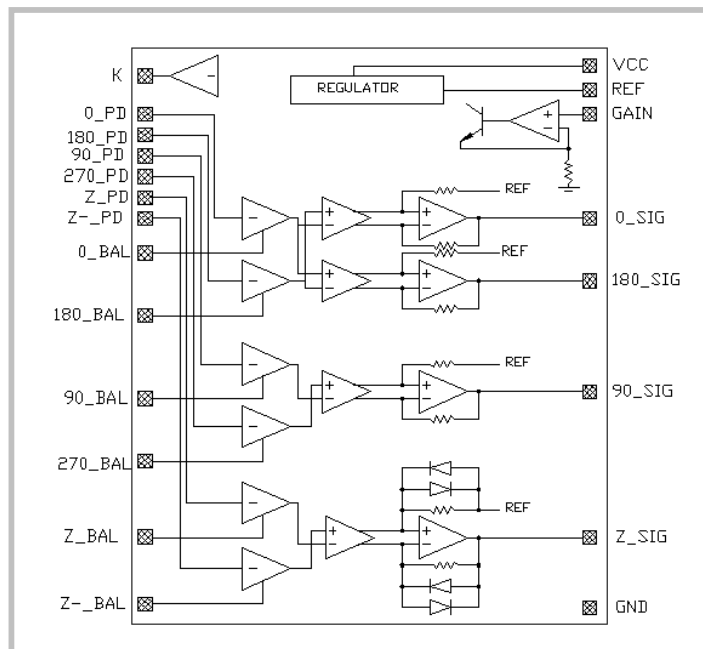
DESIGN SPECIFICATIONS

Parameter	Symbol	Min.	Max.	Units	Comments
Operating Temperature Range	T_A	-40	120	°C	
Storage Temperature Range	T_S	-55	150		
Supply Voltage Range	V_{CC}	4.5	5.5	V	

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{CC}=5V$, $T_A = 25^\circ C$, $I_{OFFSET} = 1.5\mu ADC$, and $I_{IN} = 750nA_{(P-P)} @ 100KHz$.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current	I_{CC}	--	11.3	15.8	mA	$V_{CC}=5.5V$
REF Voltage	V	--	2.6	--	V	
K (photodiode cathode bias)	V	1.14	1.25	1.35	V	
0_SIG, 90_SIG, 180_SIG, & Z_SIG output voltage, peak to peak	V_{P-P}	--	750	--	mV	GAIN=1.25V and default input conditions
0_SIG, 90_SIG, 180_SIG, & Z_SIG output voltage, DC offset	V_{OFFSET}	--	2.6	--	V	GAIN=1.25V and default input conditions



Block Diagram

Preliminary Data – Subject to Change

Pin Descriptions

Pin #	Pin Name	Description/Use
1,2,3,4	0°,180°, 90°, 270° PHOTODIODE	Inputs for the photodiode signals from the data channels
5,6	Z+, Z- PHOTODIODE	Inputs for the photodiode signals from the index channel
7,8,9,10	0°,180°, 90°, 270° BALANCE	Adjust pins for data signal balancing via resistor to ground
11,12	Z+, Z- BALANCE	Adjust pins for index signal balancing via resistor to ground
13,14	N.C.	
15	GND	Return for supply voltage
16	Z_SIG	Index channel amplified sinewave output, level shifted
17,18,19	90°_SIG, 180°_SIG, 0°_SIG	Data channel amplified sinewave output, level shifted
20	REF	Output of internal reference voltage (to feed forward as comparator threshold set point)
21	GAIN	Input for voltage controlled amplifiers, 0-2.5V
22	VCC	Supply voltage input, 5V
23	N.C.	
24	K	Output of internal bias voltage for cathode of photodiodes

Preliminary Data – Subject to Change